AMENDED CLAIMS
[received by the International Bureau on January 17, 2005 (17.01.05);
original claims 1-21 amended; original claim 22 cancelled (6 pages)]

CLAIMS

1. (Amended) A processing device, comprising:

a reconfigurable circuit (12) allowing change in function;

a first path portion (24) transmitting an output of said reconfigurable circuit (12) as an input to said reconfigurable circuit (12);

a setting portion (14) supplying setting data (40) for configuring an intended circuit in said reconfigurable circuit (12);

a control portion (18) controlling said setting portion (14) such that a plurality of setting data are successively supplied to said reconfigurable circuit (12), so that an output of a circuit configured on said reconfigurable circuit (12) in accordance with one setting data is supplied to an input of a circuit configured in accordance with next setting data through said first path portion (24); and

an internal state holding circuit (20) receiving an output of said reconfigurable circuit (12),

said internal state holding circuit (20) being connected to said first path portion (24);

said device further comprising:

a memory portion (27) storing in a prescribed area an output of a circuit configured on said reconfigurable circuit (12) in accordance with said one setting data; and

a second path portion (29) transmitting the output of the circuit configured on said reconfigurable circuit (12) stored in said prescribed area of said memory portion (27) as an input to a circuit configured in accordance with the next setting data.

2. (Amended) The processing device according to claim 1, wherein

said internal state holding circuit (20) operates at a higher speed than said memory portion (27).

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3. (Amended) The processing device according to claim 1, wherein said setting portion (14) successively supplies a plurality of setting data to said reconfigurable circuit (12), so that one circuit is formed as a whole.

4. (Amended) The processing device according to claim 1, wherein said plurality of setting data (40a ~ 40d) represent a plurality of divided circuits (A~D) obtained by dividing one circuit (42).

5. (Amended) The processing device according to claim 1, wherein said reconfigurable circuit is configured as a combinational circuit (50, 52).

6. (Amended) The processing device according to claim 1, further comprising: an output circuit (22) receiving an output of said reconfigurable circuit (12), said output circuit (22) providing the output of said reconfigurable circuit (12) when said reconfigurable circuit (12) is configured a plurality of times by said setting portion (14).

7. (Amended) The processing circuit according to claim 1, further comprising: a switching circuit (28) switching between the input from said second path portion (29) and an external input, to be an input to said reconfigurable circuit (12).

8. (Amended) The processing device according to claim 1, wherein said reconfigurable circuit (12) includes a plurality of logic circuits (50) each capable of selectively executing a plurality of operation functions, and a connecting portion (52) allowing setting of connection relation among the logic circuits; and said setting portion (14) sets the functions and said connection relation of said logic circuits (50).

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9. (Amended) The processing device according to claim 8, wherein said logic circuit (50) is an arithmetic logic circuit (ALU) capable of selectively executing a plurality of multi-bit operations.

10. (Amended) A processing method, comprising the steps of: configuring a plurality of divided circuits (A~D) obtained by dividing one circuit (42) on a reconfigurable circuit (12); feeding back an output of one divided circuit to an input of a next divided circuit to execute an operation in the divided circuits; and taking out an output from the last configured divided circuit.

11. (Amended) An integrated circuit device, comprising:
a reconfigurable circuit (12) allowing change in function;
a path portion (24) connecting an output of said reconfigurable circuit (12) to an input of said reconfigurable circuit (12); and
a setting portion (14) supplying setting data (40) for configuring an intended circuit on said reconfigurable circuit (12).

12. (Amended) A processing device, comprising:
a reconfigurable circuit (12#a) allowing change in function and connection relation;
a setting portion (14#) storing setting data representing a divided unit forming a part of an intended circuit and supplying the setting data to said reconfigurable circuit (12#a); and
a control portion (18) controlling said setting portion (14#) such that a plurality of setting data are successively supplied to said reconfigurable circuit (12#a) to configure said intended circuit; wherein
said reconfigurable circuit (12#a) has at least one state holding circuit (52#a)

holding an internal state;

said reconfigurable circuit (12#a) is divided, by an arrangement of said state holding circuit (FT), into a plurality of stages of reconfigurable units; and

said control portion (18) controls said setting portion (14#) such that when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow.

13. (Amended) The processing device according to claim 12, wherein

said reconfigurable circuit is divided, by an arrangement of N state holding circuit (FT), into (N+1) stages of reconfigurable units;

said control portion (18) controls said setting portion (14#) such that at one time point, setting data of a divided unit configuring an intended circuit is supplied to said reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit,

controls said setting portion (14#) such that at a next time point, setting data of a next divided unit configuring said intended circuit is supplied to said reconfigurable unit between (i+1)th state holding circuit and (i+2)th state holding circuit in accordance with the process flow, and controls said setting portion (14#) such that setting data of a divided unit configuring a different intended circuit is supplied to said reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit (52#a).

14. (Amended) The processing device according to claim 12, wherein

said reconfigurable circuit (12#a) is divided, by the arrangement of N state holding circuits (FT), into N stages of reconfigurable units;

said control portion (18) controls said setting portion (14#) such that at one time point, setting data of a divided unit configuring an intended circuit is supplied to said reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit,

controls said setting portion (14#) such that at a next time point, setting data of a

next divided unit configuring said intended circuit is supplied to said reconfigurable unit between (i+1)th state holding circuit and (i+2)th state holding circuit in accordance with the process flow, and controls said setting portion (14#) such that setting data of a divided unit configuring a different intended circuit is supplied to said reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit;

said device further comprising

a path portion (24) for providing an input from the N-th state holding portion to the first stage of reconfigurable units.

15. (Amended) The processing device according to claim 12, wherein said reconfigurable unit is configured as a combinational circuit (50, 52#a).

16. (Amended) The processing device according to claim 12, further comprising:

an output circuit (22) receiving an output of said reconfigurable circuit (12#a),

said output circuit (22) providing the output of said reconfigurable circuit (12#a) when said reconfigurable circuit (12#a) is configured a plurality of times by said setting portion (14#).

17. (Amended) The processing circuit according to claim 12, further comprising:

an internal state holding circuit (20) receiving an output of said reconfigurable circuit (12#a); and

a first path portion (24) inputting the output signal held by said internal state holding circuit (20) to the first stage of reconfigurable units.

18. (Amended) The processing device according to claim 17, further comprising:

a memory portion (27) storing in a prescribed area an output of said reconfigurable circuit (12#a) in accordance with a setting data; and

a second path portion (29) transmitting the output of the circuit configured on said reconfigurable circuit (12#a) stored in said prescribed area of said memory portion (27) as an input to a circuit configured in accordance with the next setting data.

19. (Amended) The processing circuit according to claim 18, further comprising:

a switching circuit (28) switching between the input from said second path portion (29) and an external input, to be an input to said reconfigurable circuit (12#a).

20. (Amended) The processing device according to claim 12, wherein

said reconfigurable unit includes a plurality of logic circuits (50) each capable of selectively executing a plurality of operation functions, and a connecting portion (52#a) allowing setting of connection relation among the logic circuits; and

said setting portion (14#) sets the functions and said connection relation of said logic circuits (50).

21. (Amended) The processing device according to claim 20, wherein

said logic circuit (50) is an arithmetic logic circuit (ALU) capable of selectively executing a plurality of multi-bit operations.

22. (Cancelled)